APPLICATION OF QUANTITATIVE METHODS FOR RELIABILITY TESTING OF A NUCLEAR POWER PLANT DIGITAL ROD POSITION INDICATION DIAGNOSTIC SYSTEM

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ABSTRACT

Obsolescence, aging, reliability, and performance issues are driving nuclear facilities to replace conventional analog Instrumentation and Control (I&C) systems with digital technologies. In addition, the designs of the next generation of nuclear reactors, including Small Modular Reactors (SMRs), will incorporate digital I&C for most, if not all, of their safety and non-safety related functions. As part of an on-going research and development (R&D) effort under the auspices of the U.S. Department of Energy (DOE), Analysis and Measurement Services Corporation (AMS) is developing a platform to provide automated testing of digital I&C systems and create a standard method of evaluation for reliability assessments. This hands-on R&D effort has produced a Software Reliability Tester (SRT), which is a set of software and hardware tools designed to automate the testing of digital I&C systems to measure and quantify how well the systems perform under normal operating conditions and in the presence of faults. Furthermore, the SRT provides the foundation for a practical tool to automate verification and validation (V&V) activities and reduce the amount of testing time of digital I&C systems. When combined with its capabilities of integrating both reliability and fault tolerance quantification, the SRT can be used to ensure that digital I&C implementations are both safe and cost-effective for the nuclear industry.

This paper describes the application of the SRT to perform V&V of a new Digital Rod Position Indication (DRPI) diagnostic system. The DRPI diagnostic system is a digital system that monitors the rod address and rod position data bus voltages of typical DRPI systems in nuclear power plants to detect and diagnose faults. For this application, the SRT was configured to exercise the inputs of the DRPI diagnostic system, and test cases were generated for common system faults such as address and data bit errors, bus voltage, and timing problems. These test cases were applied by the SRT hardware as voltage inputs to the DRPI diagnostic system and the outputs were compared to expected values generated by a model of the DRPI diagnostic system.

Included in the paper is a description of the overall design of the SRT including the hardware and software architectures. Methodologies for automating test cases are also described. V&V using the SRT demonstrates the benefits of automated testing and qualification to provide a quantitative assessment of reliability and cost effective implementation of digital I&C in existing and next generation nuclear power plants.

Key Words: nuclear instrumentation and control, digital I&C, reliability, fault tolerance, verification and validation

1 INTRODUCTION

Digital I&C systems offer significant advantages for use in nuclear power plant (NPP) applications, including more accurate and stable measurements and the ability to improve diagnostics capability and system reliability [1]. However, the adoption of digital I&C systems has not progressed as quickly in U.S. nuclear facilities as expected for a variety of reasons, including regulatory concern about common cause failures (CCFs), questions regarding quantification of the reliability of software-based products, and uncertainty about the validity of software verification and validation (V&V) tools and effectiveness of software Quality Assurance (QA) procedures. While a significant number of safety-related and important-to-safety digital systems or components have been installed in operating NPPs over the last 20 years, 38 operating plants have reported potential and actual CCFs in many of these systems [2]. Experience in the nuclear industry has shown that reliance on qualitative, as opposed to quantitative, software QA processes often leads to high development and implementation costs, especially for safety-related digital systems [2]. Thus, the nuclear industry needs state-of-the-art tools to provide performance-based evidence of how well software-based equipment executes its intended functions under normal operation (reliability) and in the presence of faults (fault tolerance).

This paper describes work being conducted at Analysis and Measurement Services Corporation in development of a Software Reliability Tester (SRT) that will provide a means to quantify the reliability and fault tolerance of digital I&C systems used in nuclear facilities (Figure 1). Software reliability for a digital I&C system has been defined as the probability that a software-based digital system will successfully perform its intended function for all conditions under which it is expected to respond, upon demand, with no unintended functions that might affect system safety [3]. The SRT is comprised of hardware and software that will exercise digital equipment inputs and compare the outputs to expected values to quantify system reliability. Incorporation of fault injection techniques enables the SRT to evaluate the robustness of digital I&C in the presence of abnormal conditions. The integration of quantitative reliability and fault tolerance measures will provide the nuclear industry with an innovative and systematic approach to digital I&C qualification. This will enable safer, more reliable, and more cost-effective implementations of a broad spectrum of digital I&C equipment in existing and next generation nuclear facilities.

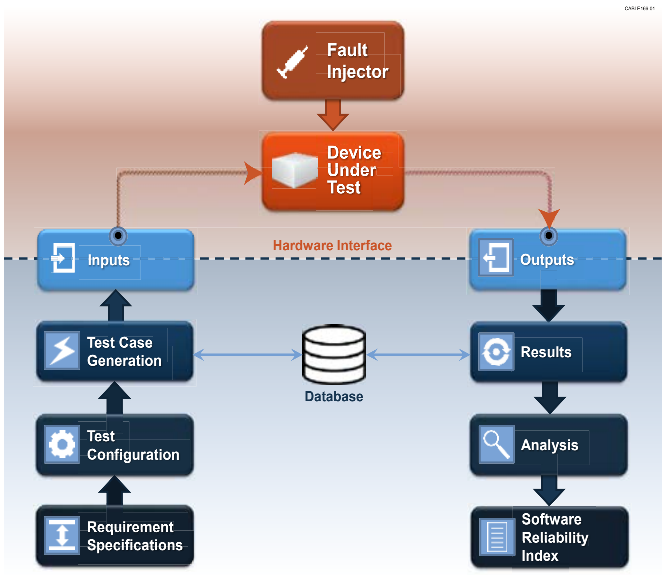


Figure 1. Design of the Software Reliability Tester

2 BACKGROUND

Software reliability assessment involves determining "the probability that software will not cause the failure of a system for a specified time under specified conditions" [4]. Risk-based methods use a combination of factors such as development processes, theoretical failure models, operational profiles, past failure rates, and engineering judgment to derive a probability of failure. Test-based methods include black, gray, and white box testing [5]. Black box testing requires little knowledge of the underlying system and tests the system based on its intended functionality. White and gray box testing require a more detailed knowledge of the system and can be used to test source code or individual functions at a lower level.

Fault tolerance is defined as "the ability of a system or component to continue normal operation despite the presence of hardware or software faults" [3]. Fault injection testing aims to evaluate the fault tolerance of a system by introducing deliberate faults and observing the system's behavior, potential design flaws, and limitations that likely would not become known until a system was deployed. Thus, fault injection testing serves as a form of accelerated testing of the fault tolerance of the system under test [6]. The behavior of I&C equipment in abnormal conditions must be well understood before deployment in the nuclear industry. Therefore, fault tolerance testing is particularly important, especially in safety-related applications.

The reliability techniques implemented in the SRT to date have focused heavily on black and gray box testing [7]. Likewise, fault injection testing methods focused on electromagnetic interference/radio frequency interference (EMI/RFI) and electrostatic discharge (ESD) testing [8].

The SRT has been used for validation testing of a new Digital Rod Position Indication (DRPI) diagnostic system (DDS). This system adds complexity in a significant increase in channel density, new communication structure for retrieving data from the device, and a knowledge of the data patterns utilized in the DRPI and DDS systems, thereby making this more of a white box approach.

3 SRT DEVELOPMENT

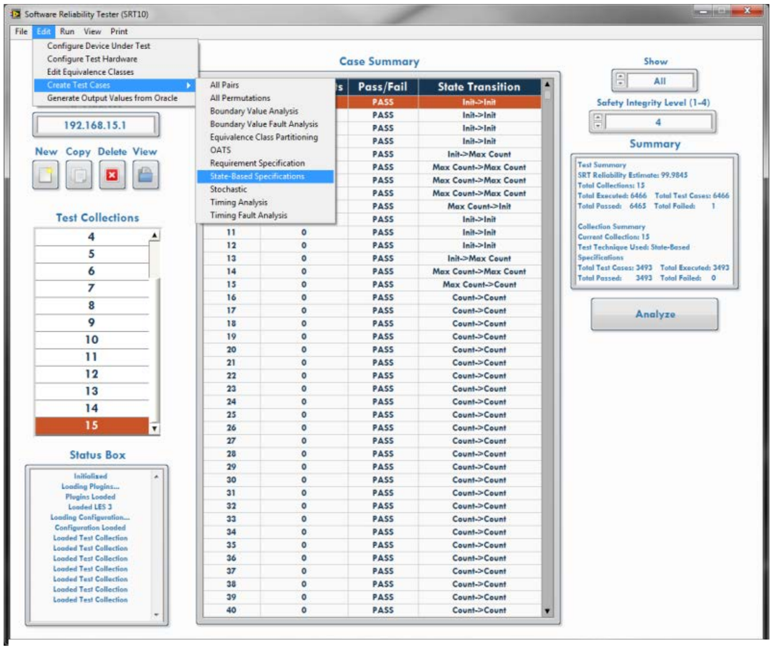
The overall design of the SRT is previously shown in Figure 1. The SRT is designed to use the requirement specifications of the device under test (DUT) to create various test cases that are applied to the DUT. Several different types of test case generation methods were selected for implementation for reasons such as their simplicity (all permutations, boundary value analysis, and stochastic testing), their common acceptance by the software engineering industry (all pairs, requirements specifications, orthogonal array testing strategy, and state-based specifications), or their usefulness to serve as bases for other methods (equivalence class partitioning) [9-11].

3.1 SRT Implementation and Operation

The SRT includes software reliability and fault tolerance tools designed to automate both the test case creation process and the testing of a digital system. The SRT was developed with a modular software architecture which allows testing techniques to be developed as plugins for the main program. The main screen (Figure 2) provides the interface to all the functionality provided by the SRT. From the main screen, a test can be configured, created, and executed.

Reliability and fault tolerance testing is performed with the following process. First, the Device Under Test (DUT) is configured within the SRT software. This involves defining the inputs and outputs of the system, including the input data type, e.g. double-precision floating point, 32-bit signed integer, Boolean, etc. This information is sent to the Hardware Abstraction Layer (HAL), as described in the next section.

After configuring the DUT, test cases may be loaded from an externally generated file, or generated manually or automatically using the SRT test case generation methods. Using the selected test cases, the DUT is then tested and the pass/fail results are reported. The individual test case



192.168.15.1

Show: All

Safety Integrity Level (1-4): 4

Test Collections
4
5
6
7
8
9
10
11
12
13
14
15

	s	Pass/Fail	State Transition
		PASS	Init->Init
		PASS	Init->Init
		PASS	Init->Init
		PASS	Init->Init
		PASS	Init->Max Count
		PASS	Max Count->Max Count
		PASS	Max Count->Max Count
		PASS	Max Count->Max Count
		PASS	Max Count->Init
		PASS	Init->Init
11	0	PASS	Init->Init
12	0	PASS	Init->Init
13	0	PASS	Init->Max Count
14	0	PASS	Max Count->Max Count
15	0	PASS	Max Count->Count
16	0	PASS	Count->Count
17	0	PASS	Count->Count
18	0	PASS	Count->Count
19	0	PASS	Count->Count
20	0	PASS	Count->Count
21	0	PASS	Count->Count
22	0	PASS	Count->Count
23	0	PASS	Count->Count
24	0	PASS	Count->Count
25	0	PASS	Count->Count
26	0	PASS	Count->Count
27	0	PASS	Count->Count
28	0	PASS	Count->Count
29	0	PASS	Count->Count
30	0	PASS	Count->Count
31	0	PASS	Count->Count
32	0	PASS	Count->Count
33	0	PASS	Count->Count
34	0	PASS	Count->Count
35	0	PASS	Count->Count
36	0	PASS	Count->Count
37	0	PASS	Count->Count
38	0	PASS	Count->Count
39	0	PASS	Count->Count
40	0	PASS	Count->Count

```
Test Summary
SRT Reliability Estimate: 99.9845
Total Collections: 15
Total Executed: 6466    Total Test Cases: 6466
Total Passed:    6465   Total Failed:       1

Collection Summary
Current Collection: 15
Test Technique Used: State-Based
Specifications
Total Test Cases: 3493   Total Executed: 3493
Total Passed:      3493  Total Failed:     0
```

```
Initialized
Loading Plugins...
Plugins Loaded
Loaded LES 3
Loading Configuration...
Configuration Loaded
Loaded Test Collection
Loaded Test Collection
Loaded Test Collection
Loaded Test Collection
Loaded Test Collection
Loaded Test Collection
Loaded Test Collection
```

Figure 2. Prototype SRT Software

results, including the inputs, outputs, and expected and measured output values, are also accessible. In the current phase of development, the SRT is capable of directly testing software reliability with some communication with external fault injection/fault tolerance testing software.

3.2 Hardware Abstraction Layer

The SRT hardware interface provides the means to generate the input signals to be applied to a DUT and measure the resulting responses. The hardware interface is a combination of two components: data acquisition/generation equipment and a software module known as the HAL. As illustrated in Figure 3, the HAL performs four major functions: (1) SRT communication, (2) hardware input and output mapping to DUT channels, (3) DUT channel configuration, and (4) DUT communication.

When the testing begins, hardware input information is sent to the DUT from the SRT via the hardware interface. The outputs are then measured to see their response to the given input cases. This output data is then returned to the SRT where it is stored in a database. Once the testing is complete an analysis is performed and the results are quantified.

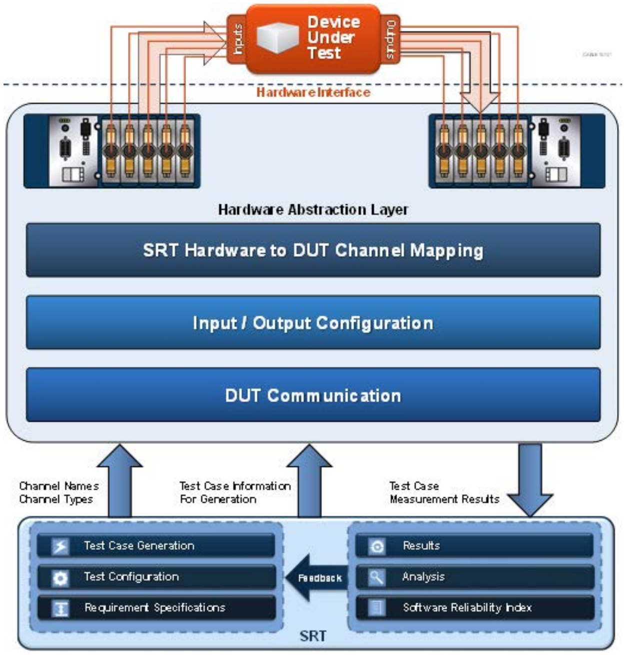


Figure 3. SRT Architecture with Hardware Interface

4 DRPI DIAGNOSTICS SYSTEM TESTING

The design of many existing Pressurized Water Reactors (PWRs) incorporate a Digital Rod Position Indication (DRPI) system to monitor the positions of the control and shutdown rods within the reactor. DRPI systems continuously sense the position of each of the control and shutdown rods via coil stacks that are mounted on the rod control housing above the reactor. Each coil stack consists of 21 individual coils, which are excited with an alternating current (AC) voltage as shown in Figure 4. When a control or shutdown rod shaft enters a coil, the AC current through the coil changes. The analog electronics in the existing DRPI system detect the change in current and set a digital bit for each coil in the coil stack. These digital bits are transmitted to the control room to provide the rod position.

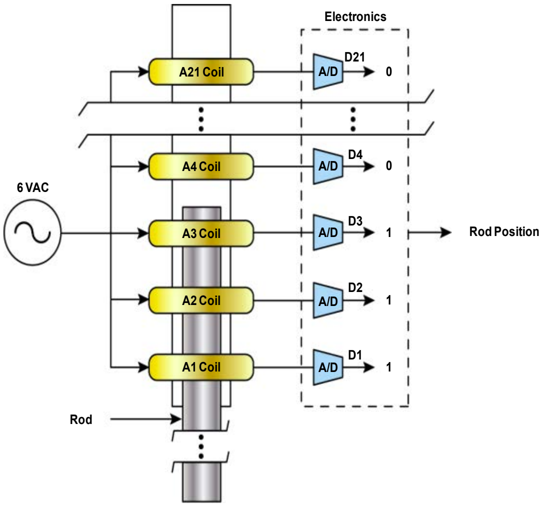


Figure 4. Example of Existing DRPI System

The DDS connects to the DRPI address and data bus that communicates between the DRPI data cabinet in containment and the DRPI display cabinet in the control room (Figure 5). It receives the digital (Gray Code) signals, verifies proper voltage level and timing, converts address and data to Rod ID and Rod Position, logs data when an error occurs, stores rod drop data and calculates rod drop times, and transmits the diagnostic data to the DDS Master Controller. This paper reflects the details of testing one component of the DDS, the DRPI Gray Code module (EGC3) and the results and findings that were produced.

Testing of the EGC3 adds significant complexity compared to the previous devices tested by the SRT. First, the number of channels of the EGC3 system is significantly greater than other DUTs previously tested with the SRT. Next, the DRPI digital bus data has a specific pattern, and knowledge of this pattern is necessary to properly test the system. This makes the approach more white box in nature than previous testing. Finally, previous testing utilized only digital inputs and outputs whereas the EGC3 consists of analog inputs and a digital network communication output. This requires more complex communication between the SRT and the EGC3 system during testing.

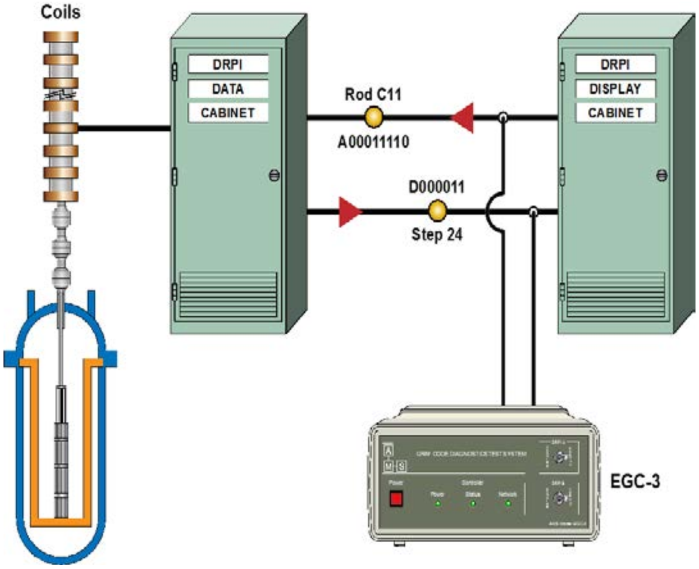


Figure 5. Schematic of DRPI Diagnostic System

The EGC3 is designed to acquire rod positon data in binary Gray Code. The SRT has been used to test this component. Testing of the EGC3 consisted of 27 inputs, each representing a voltage value to be sent to the EGC3 for data acquisition. Analog output modules were used with the HAL to generate the voltage inputs for the Gray Code testing as shown in Figure 6. Each output of the HAL was mapped to an EGC hardware input. Each voltage input represents a single bit, and each test case has 7 bits for the A address, 7 bits for the B address, 6 bits for the A data, 6 bits for the B data, and 1 trigger bit.

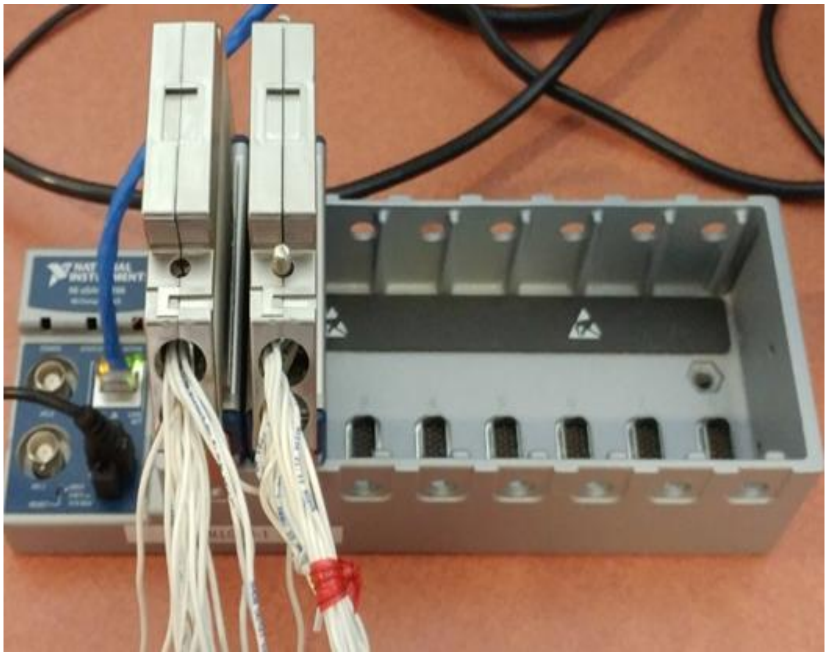


Figure 6 HAL Equipment Used for EGC3 Testing

The data sections each contain 6 bits – 5 for the position and 1 parity bit. The parity bit is used by the DRPI system to detect single bit communication errors and is determined by the number of 1's in the position and address bits. If the number is odd, the parity bit is 1. Otherwise, the parity bit is set to 0. The positions are determined by counting sequentially in binary Gray Code, and some examples of the corresponding Gray Codes are shown in Table I. In addition to the 27 inputs, the EGC3 returns a single unsigned 32-bit integer output via a network stream using TCP/IP. The format of the information encoded in the 32-bit integer message is shown in Table II.

Table I. DRPI Gray Code Binary Data and Associated Rod Positions

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A Position	B Position
0	0	0	0	0	0	6
0	0	0	0	1	12	18
0	0	0	1	1	24	30
0	0	0	1	0	36	42
:	:	:	:	:	:	:
1	1	0	1	0	228	228

Table II. Bit Layout of 32-bit Unsigned Integer Returned from EGC3

Bit	Input	Bit	Input	Bit	Input	Bit	Input
1	Data B0	9	Addr B0	17	Data A0	25	Addr A0
2	Data B1	10	Addr B1	18	Data A1	26	Addr A1
3	Data B2	11	Addr B2	19	Data A2	27	Addr A2
4	Data B3	12	Addr B3	20	Data A3	28	Addr A3
5	Data B4	13	Addr B4	21	Data A4	29	Addr A4
6	Data B5p	14	Addr B5	22	Data A5p	30	Addr A5
7	0	15	Addr B6	23	0	31	Addr A6
8	Trigger	16	1	24	Trigger	32	0

There are 128 possible values of the 7 address bits. For the 6 data bits, there are 20 valid Gray Codes. Thus, there are 128 x 20 = 2560 total test cases necessary for full coverage of the valid input space of the EGC3. A test of all of the valid input space is therefore practical for Gray Code testing. However, since there are 6 bits for the data there are 64 possible values for data, including invalid bits. Thus, there are 128 x 64 = 8,192 possible values that include both valid and invalid inputs. Additionally, because it is possible for the A channels and B channels to receive different data, the input space is increased dramatically to 8,192 x 8,192 = 67,108,864. Therefore, the testing was scoped to generate test cases for all the valid input space of the EGC3 system as well as select representative sets of invalid inputs.

After test case generation, the test cases were saved in a file for the SRT to read. From this file, the SRT sent the test cases one-by-one to the HAL via network stream. When the HAL received a test case, it converted the 27 bits into voltages where True = 5.0 volts and False = -5.0 volts and then output them to the EGC3 inputs. The EGC3 then measured the voltages, converted them into digital bits, and sent the response back to the HAL in the form of an unsigned 32-bit integer over a network stream. Then, the HAL received the digital data and sent it the SRT over another network stream. At the same time, these test cases were sent to the EGC software model to generate expected results. After the SRT received the values from both the software model and the HAL, it compared the two values and logged the test case as pass or fail. For the test cases that resulted in a sequential ordering of valid inputs, as shown in Figure 7, were generated using a requirements specification approach. The results of the 2560 test cases generated using the requirement specification method are shown in Figure 8. For this testing, every test case succeeded and the hardware performed as expected. Note that the SRT Reliability Estimate is 100 in the summary box on the right of Figure 8 for this test, and the total failed cases is 0. This means that given the generated inputs the EGC3 measured output matched the expected output from the model for all 2560 test cases.

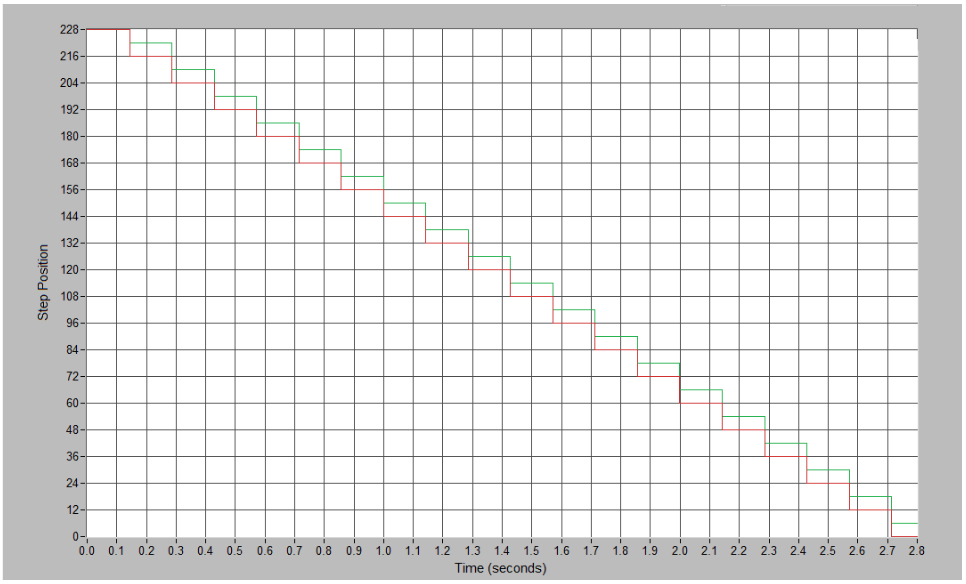
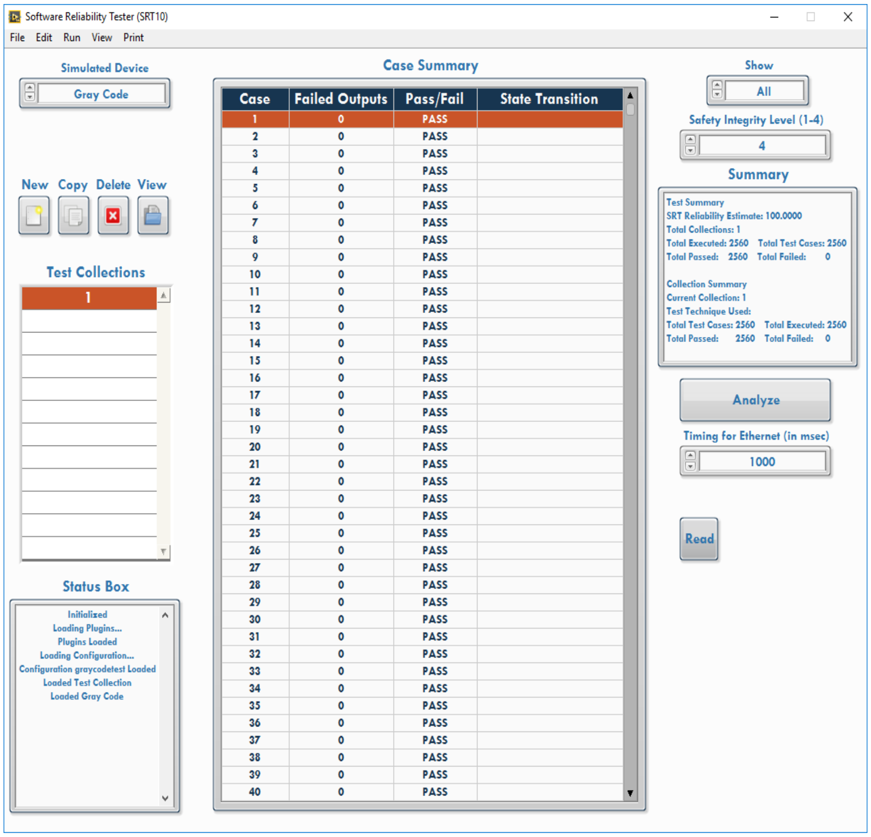


Figure 7. Gray Code Test Signal sent to DUT



Case Summary

Case	Failed Outputs	Pass/Fail	State Transition
1	0	PASS	
2	0	PASS	
3	0	PASS	
4	0	PASS	
5	0	PASS	
6	0	PASS	
7	0	PASS	
8	0	PASS	
9	0	PASS	
10	0	PASS	
11	0	PASS	
12	0	PASS	
13	0	PASS	
14	0	PASS	
15	0	PASS	
16	0	PASS	
17	0	PASS	
18	0	PASS	
19	0	PASS	
20	0	PASS	
21	0	PASS	
22	0	PASS	
23	0	PASS	
24	0	PASS	
25	0	PASS	
26	0	PASS	
27	0	PASS	
28	0	PASS	
29	0	PASS	
30	0	PASS	
31	0	PASS	
32	0	PASS	
33	0	PASS	
34	0	PASS	
35	0	PASS	
36	0	PASS	
37	0	PASS	
38	0	PASS	
39	0	PASS	
40	0	PASS	

Summary

```
Test Summary
SRT Reliability Estimate: 100.0000
Total Collections: 1
Total Executed: 2560    Total Test Cases: 2560
Total Passed:    2560   Total Failed:      0

Collection Summary
Current Collection: 1
Test Technique Used:
Total Test Cases: 2560   Total Executed: 2560
Total Passed:     2560   Total Failed:   0
```

Status Box

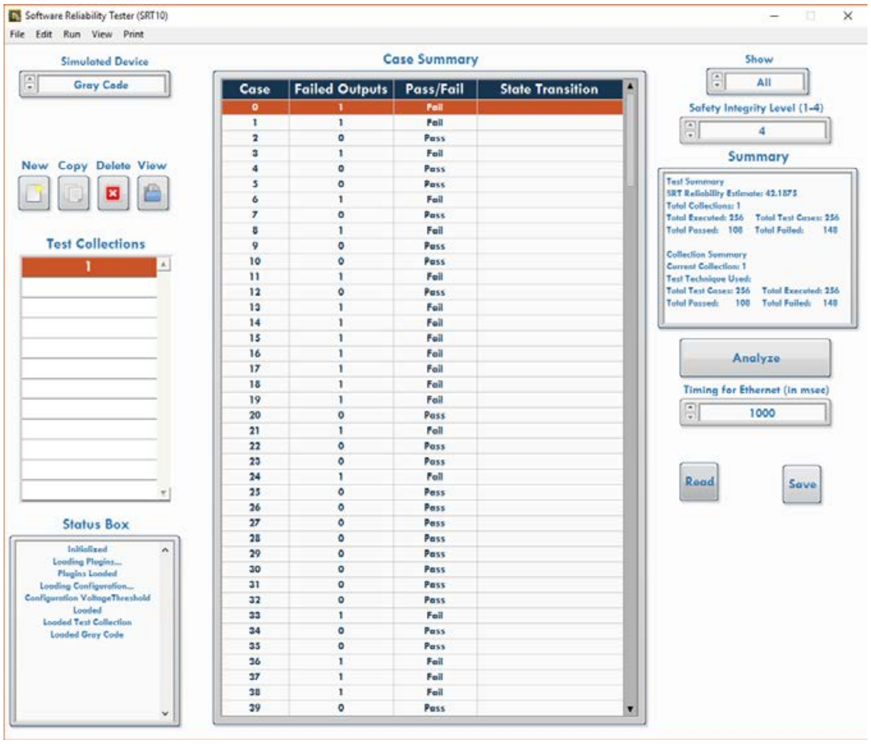
```
Initialized
Loading Plugins...
Plugins Loaded
Loading Configuration...
Configuration graycodetest Loaded
Loaded Test Collection
Loaded Gray Code
```

Figure 8. Test of EGC3 System with no Fault Injection

Testing was also conducted with a stochastically ordered set of the valid input space test cases. During normal operation of the system, the data would be presented sequentially. However, the DDS needs to be able to handle the situation where data is not changed in a sequential order without error. The stochastic testing of the 2560 valid test cases was completed with an SRT Reliability Estimate of 100. This means that the DDS is handling the changing of inputs in a non-sequential order. Additionally, the SRT has been used for testing of the DDS with test cases containing known faults such as invalid address bits, incorrect parity bits, and false data bits. In each of these known fault conditions the DDS operated as expected.

Test cases have shown that the EGC3 responds appropriately under expected operating and fault conditions. However, how the EGC3 responds when given unexpected fault conditions also needs to be evaluated. One example of an unexpected fault is when voltage values on the bus are at or near digital ON/OFF threshold levels. Under normal conditions the voltage on each digital line will be sufficiently above the digital threshold that electrical noise will not affect the reading. However, if the ON voltage output experienced some component degradation and the ON output value was low, small levels of electrical noise could cause the EGC3 to incorrectly read the output as ON/OFF transitions. This scenario has been tested using the SRT with test cases by setting the input to the EGC3 just above the ON/OFF threshold level. The results showed that there was enough noise in the current test setup to alter the EGC3 input during many of the tests as displayed in Figure 9. Note that the observed SRT Reliability Estimate is 42.1875% for this testing.

Another possible unexpected fault condition would be the DRPI system sending Gray Code data faster than the EGC3 is able to process. This was simulated by slowing the sample rate of the EGC3 such that some test cases are missed by the EGC3, and the SRT successfully recognized the errors. The ability for the SRT to diagnose the responses of EGC3 type systems to expected and unexpected faults delivers tremendous value to commercial vendors during the development of digital I&C equipment. The SRT results allow vendors to catch and resolve design issues during the development process thereby increasing the systems reliability and greatly reducing development costs.



Simulated Device: Gray Code

Test Collections: 1

Status Box

Initialized
Loading Plugins...
Plugins Loaded
Loading Configuration...
Configuration VoltageThreshold Loaded
Loaded Test Collection
Loaded Gray Code

Case Summary

Case	Failed Outputs	Pass/Fail	State Transition
0	1	Fail	
1	1	Fail	
2	0	Pass	
3	1	Fail	
4	0	Pass	
5	0	Pass	
6	1	Fail	
7	0	Pass	
8	1	Fail	
9	0	Pass	
10	0	Pass	
11	1	Fail	
12	0	Pass	
13	1	Fail	
14	1	Fail	
15	1	Fail	
16	1	Fail	
17	1	Fail	
18	1	Fail	
19	1	Fail	
20	0	Pass	
21	1	Fail	
22	0	Pass	
23	0	Pass	
24	1	Fail	
25	0	Pass	
26	0	Pass	
27	0	Pass	
28	0	Pass	
29	0	Pass	
30	0	Pass	
31	0	Pass	
32	0	Pass	
33	1	Fail	
34	0	Pass	
35	0	Pass	
36	1	Fail	
37	1	Fail	
38	1	Fail	
39	0	Pass	

Show: All

Safety Integrity Level (1-4): 4

Summary

Test Summary
SRT Reliability Estimate: 42.1875
Total Collections: 1
Total Executed: 256 Total Test Cases: 256
Total Passed: 108 Total Failed: 148

Collection Summary
Current Collection: 1
Test Technique Used:
Total Test Cases: 256 Total Executed: 256
Total Passed: 108 Total Failed: 148

Timing for Ethernet (in msec): 1000

Figure 9. Test of EGC3 System with Low 'ON' Voltage

5 FUTURE WORK

As discussed above, the DDS is a very complex multiple module system and the work herein only addressed the digital diagnostic module of the full DDS system. More work is needed to reach the channel density necessary to test the coil diagnostic module and the all DDS modules working in tandem. Furthermore, additional fault testing is needed, including testing of the system under various electromagnetic environments. Additionally, the SRT design will be made modular to allow for adaptation of equipment with additional interfaces in order to accommodate the numerous types of devices that will be tested. Finally, the design will be rigorously tested to adhere to nuclear industry regulations and guidelines prescribed for digital equipment and software.

6 CONCLUSIONS

The product of this work will give the nuclear industry a valuable resource that supports obsolescence management and mitigates many of the risks associated with digital upgrades. The primary benefits the SRT will provide are:

- an automated testing process
- independent verification and validation
- quantification of digital reliability and fault tolerance

Existing standards that are used to qualify digital systems are more focused on process-oriented evaluation than measurable, quantitative analysis. The benefits of this system help to address this gap by complementing the software lifecycle based reliability measures with quantifiable indices of software reliability and fault tolerance.

An automated testing process reduces time and money spent during costly V&V activities. The automated testing can be conducted throughout various development phases to chart progress and understand design limitations. These V&V activities are required to be carried out by independent organizations for certain levels of safety. The SRT can fill this need for digital vendors and utilities alike by providing a cheaper and more effective alternative to the methods currently in use.

7 ACKNOWLEDGMENTS

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