Implementing a control application on an FPGA Platform

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ABSTRACT

Today, many I&C system suppliers propose FPGA-based I&C platforms. In that context, EDF has set up a project to assess the use of such platforms for safety-related systems and to enhance EDF's ability to manage this technology for the upgrade of existing I&C systems or for new constructions. One aim of the project is to assess the adequacy of these platforms for the development of control functions.

This paper presents the development of a case study on a Radiy FPGA-based platform in a Hardware-In-the-Loop configuration, and the comparison with a Dymola Model-In-the-Loop and a Siemens T2000 S7 Hardware-In-the-Loop approach.

The case study is a part of the level control of steam generators of French PWR NPP. The control flow diagram uses complex analog elementary blocks coded with fixed point format for the analog values. The use of IP cores of the FPGA supplier was avoided to enable a complete mastership of the VHDL code, to provide evidence of compliance with safety-related requirements, and to allow porting this code to another FPGA platform.

The case study has highlighted the specificity of using a FPGA, and has shown that a complex control application in a FPGA-based PLC presents no major differences in precision and response time with a processor-based PLC.

Key Words: FPGA, HIL, fixed-point

1 INTRODUCTION

For many years, EDF R&D has studied the use of FPGAs in the framework of refurbishment of safety critical or safety related systems for Nuclear Power Plants. For that purpose EDF R&D has developed FPGA custom-made solutions with new electronic cards to replace an obsolete processor, or done partial renovation of I&C systems. Currently a FPGA Standard base is being set up with the IEC 62566 [1] which describes the development of HDL programmed integrated circuits for category A functions, and another Standard for categories B and C is being written. Besides, many I&C system suppliers presently propose FPGA-based platforms.

To plan including this technology in our engineering process, EDF has set up a project and selected a FPGA-based platform for evaluation. Another goal of this project is to increase the EDF knowledge on these platforms to consider the use of this technology for I&C system refurbishment or new NPPs contracts.

2 CASE STUDY

EDF R&D has two objectives:

- Prove that the use of a FPGA based I&C platform for nuclear applications is nowadays possible. And identify the use cases of a FPGA-based PLC, such as logical, analog or alarm processing.
- Assess the design process of these platforms for nuclear engineering.

In that way, a FPGA platform was selected to be tested by EDF R&D. The aim is not to assess the platform of a specific supplier but to prove that the FPGA technology as a whole is mature enough for nuclear applications.

The case study described in this paper consists in the design on that FPGA platform of a complex analog control system. The aim is to identify features of a FPGA-based PLC such as design and choice of elementary function blocks, selection of floating or fixed-point precision, simulation and tests environment.

A performance comparison with a processor-based PLC will be presented.

2.1 FPGA test platform

The FPGA-based PLC used for the tests has a lot of common points with industrial PLC based on processors. It is made up of a logic module which centralized all the user applications and communicates with several analog and digital Input / Output modules interfaced to the process. All cards have only FPGA or CPLD. The picture below describes these interfaces:

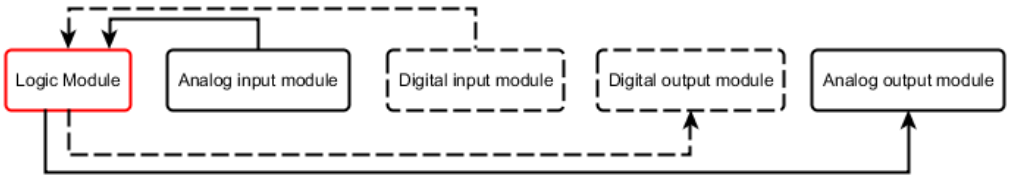

Figure 1: Interfaces between the FPGA modules

The platform is divided into two parts: the Platform Logic and the Application Logic.

The Application Logic is developed by the user, and uses services given by the Platform Logic (use of Input / Output Cards, setting the status of the system).

The Platform Logic is developed by the supplier, and manages the hardware of the I/O modules and the Logic Module. For instance this layer checks the hardware, collects data from inputs modules and sets outputs from data given by the application logic. It incorporates a framework for the Application Logic.

For early error detection, the Platform Logic duplicates the Application Logic and encodes all data path between components. These features are imperceptible for the user.

2.2 The control system

The controlled process system is in charge of the water supply of the four steam generators of the 1300 MW French Nuclear Power Plants. This system has to maintain the level of those four steam generators to a set point calculated from the nuclear load picture. There is only one input parameter for this control system, others inputs are from the process model.

Two control valves are linked to each steam generator:

- A low flow valve which is:
  - Controlled when the nuclear load is low
  - Fully opened otherwise
- A high flow valve which is:
  - Closed when the nuclear load is low
  - Controlled otherwise

And each steam generator has its own control system which computes the opening and closing of both high and low flow valves.

The figure 2 hereafter presents the links between the valves and steam generators.

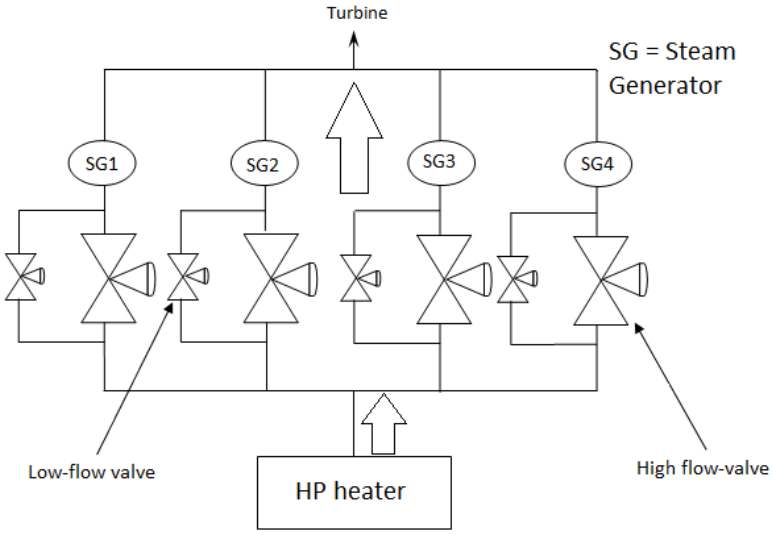

Figure 2: Process system diagram

A fixed-point precision has been chosen to make the control system, because floating point representation is generally expensive in terms of FPGA resources and the library provided by the FPGA platform supplier was a fixed-point one.

This control system is made of those fixed-points elementary blocks:

- Piecewise-linear approximation function
- Square root
- Divider
- Subtractor
- First order filter (with or without dynamic variables)

- Resize blocks (to transform the bits number between blocks with different bits size)
- Constant
- Multiplier
- Limiter (with or without dynamic variables)
- Integral
- Derivative

2.3 Design process

To design control systems it is required to use Quartus II which is a programmable logic device design software produced by Altera Intel. This software allows to make complex projects and is used for all phases of development of the control system of the FPGA such as:

- Design of modules coded in Hardware Description Language (VHDL or Verilog)
- Control system design with graphical or textual view
- Behavioral simulation of HDL modules with ModelSim (from Mentor Graphics)
- Analysis / Synthesis of the control system
- Temporal analysis (pre or post Synthesis / Place / Route)
- Place and Route phases
- Program device

In order to have a full control of the code for safety requirements and to theoretically have a possibility to port the HDL code, no IP core was used during the design process. But some parameters chosen by the supplier of the FPGA platform imply the use of some IP cores during the Analysis and Synthesis.

3 COMPARISON BETWEEN MODEL-IN-THE-LOOP AND HARDWARE-IN-THE-LOOP

3.1 Model-In-the-Loop and Hardware-In-the-Loop

Model-In-the-Loop (MIL) provides an approach to validate the control model with the use of a process model. Both of them are run in a real-time computer. This validation may be done early and tools as Simulink or Dymola are often used for this purpose. However the control model does not represent the generated code used in the controller.

Hardware-In-the-Loop (HIL) is the combination of a process model running in a real-time computer and a real Hardware equipment executing the control process. While HIL requires a true controller and more time to program it. HIL approach is much more realistic than MIL and also more practical than validation for testing the controller’s response to unusual events.

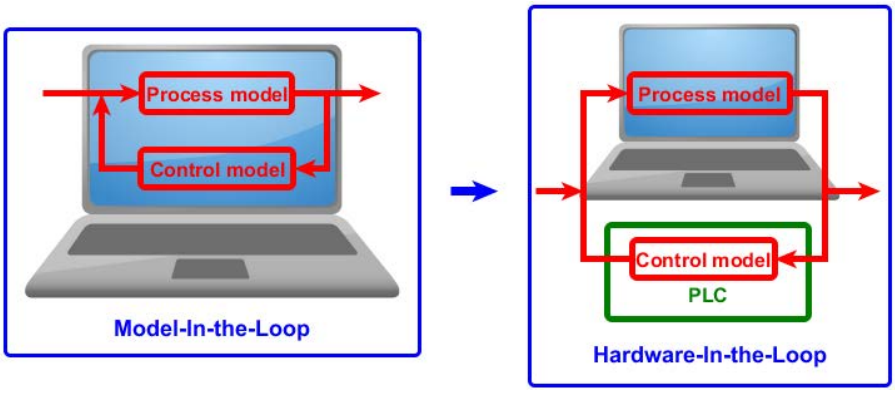

Figure 3: Model-In-the-Loop and Hardware-In-the-Loop

Three types of tests have been made with a validated process model of the NPP:

MIL or HIL	Process model	Control model	Process model processing time	Digital signal processing
MIL	Dymola (Modelica)	Dymola (Modelica language)	50ms	Floating point
HIL	Dymola (Modelica)	Real processor-based PLC used on French Nuclear NPPs	100ms	Floating point
HIL	Dymola (Modelica)	Real FPGA-based PLC	100ms	Fixed point

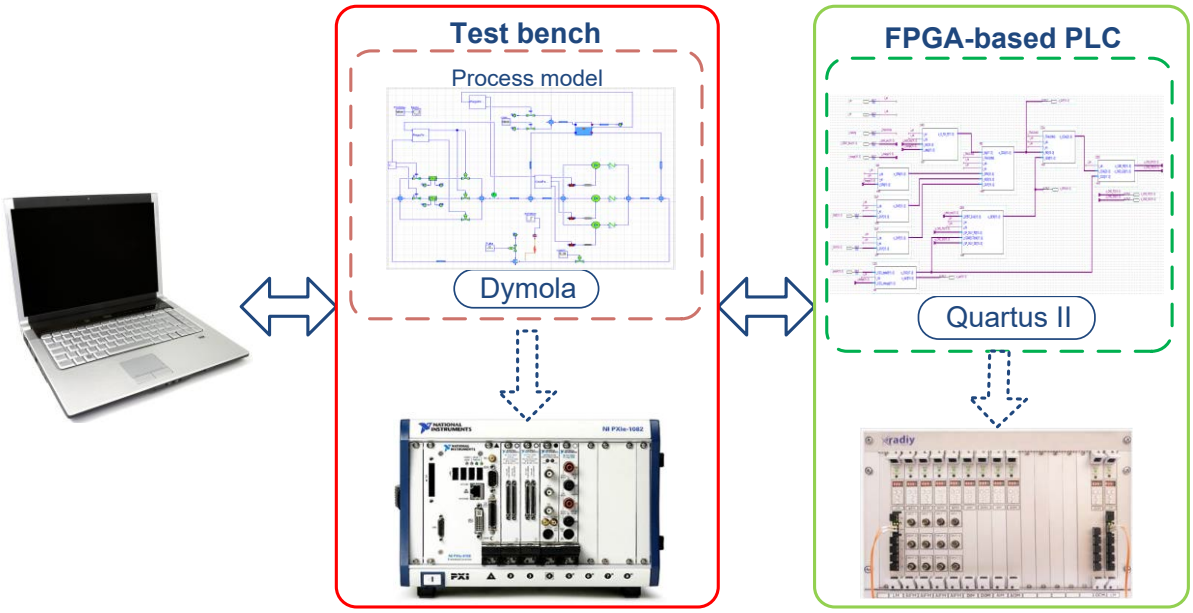

Figure 4: Hardware-In-the-Loop platform

3.2 Tests description

As the nuclear load is the only input parameter that can be changed, we made different scenarios to test the stability, response time and precision of the control system of the two PLC platforms and compared it with the reference: the MIL approach.

A drop or an increase in Nuclear Load (NL) of 1% or 2% per minute is used for the electrical grid frequency control service. And a drop or an increase in 5% represents the maximum slope allowed for this frequency control service.

Test number	Description
1	100% Nuclear Load (NL) for 40 min
2	Load drop at 1% NL / min for 40 min
3	Load drop at 2% NL / min for 20 min
4	Load drop at 5% NL / min for 8 min
5	Load increase at 1% NL / min for 40 min
6	Load increase at 2% NL / min for 20 min
7	Load increase at 5% NL / min for 8 min

Table I. Tests description

3.3 Tests results

Only scenario 2 results will be described in this paper.

The first graph represents the opening of the high flow valve which is the only control system output value that changes. A first look at this graph shows no major difference of the high flow valve control.

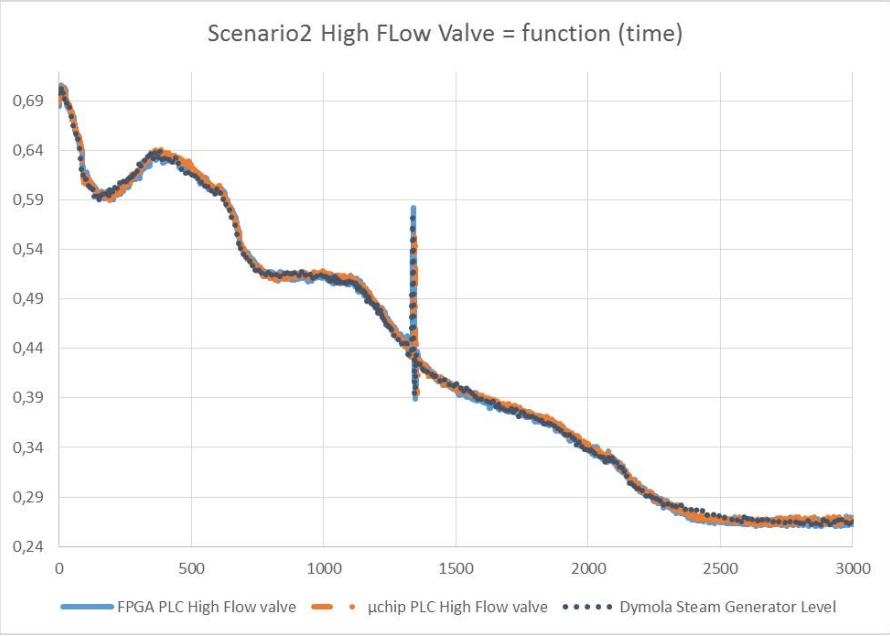

Figure 5: Scenario 2 high flow valve opening

However figure 6 called hereafter zooms in on a 50 seconds part of the figure 5 and reveals a time gap between the 3 models: a 3 seconds delay between the MIL and the FGPA HIL approach, and a 4 seconds delay between the FPGA HIL and the processor-based HIL.

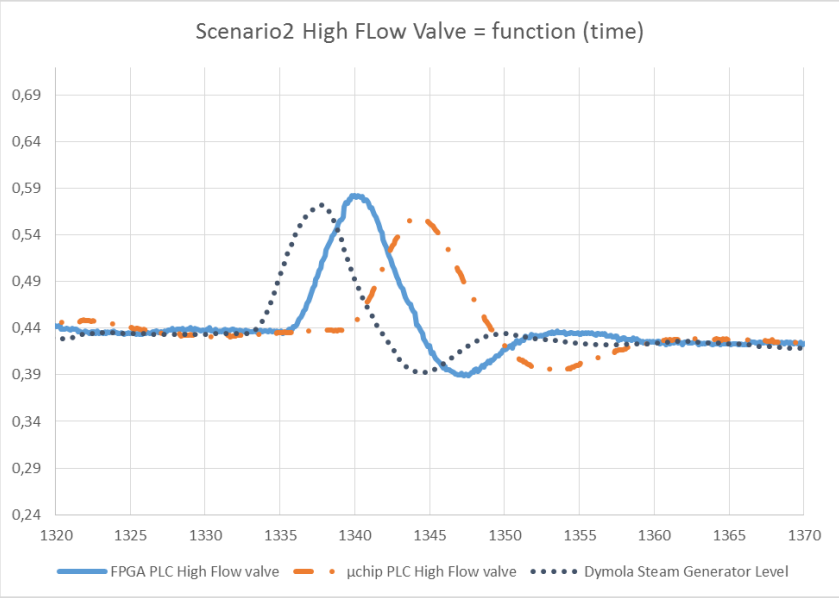

Figure 6: Scenario 2 zoom in on high flow valve opening

This slight time interval between the 3 models and a small variation of the valve opening value has clearly an impact on the steam generator response calculated in the test bench. The figure 7 mentioned below shows the steam generator level.

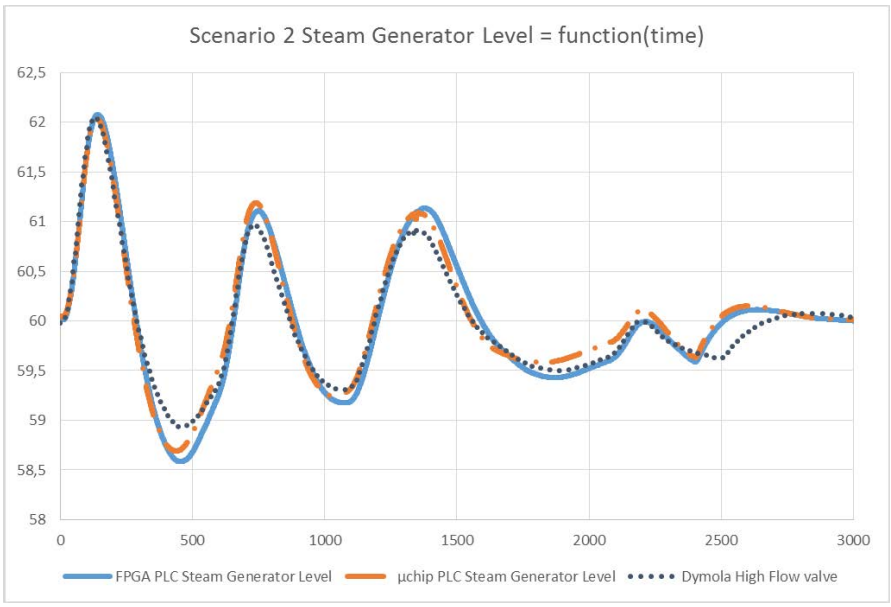

Figure 7: Scenario steam generator level

The first points to notice are the stability of the system on each MIL and HIL models and the convergence of all the models to the 60% set point. Nevertheless the longer time goes on, the more differences appear especially between the MIL model and both of the HIL approaches. There is only a small variation between the FPGA-based PLC and the processor-based PLC, while the theoretical model is a bit different. What can explain those changes may be a difference in some elementary blocks programming such as the integrator, derivative, square root, or a precision of the different acquisition I/O cards.

4 LESSONS LEARNED FROM THE TESTS

4.1 Resources consumption

To assess the capacity of the platforms to manage different application, as we have on the NNP, we have characterized the quantities to follow:

- For an FPGA based platform, we followed the number of elementary FPGA resources used by the application. Mainly we followed the number of logic bloc used;
- For software based platform, the real time constraint application are implemented in periodic task. In our platform, the most reactive task has a periodicity of 100ms. So the global load of the controller is given by the worst execution time of this periodic task. It is expressed in percent.

PLC	Logic Utilization	Real-time periodic tasks	Description
FPGA-based	28%		21 % for FPGA "System logic" and 2 x 3.5% of Application logic
Processor-based		1%	

Table II. Comparison between the two PLCs

The use of the Quartus II CAD tool allows to display a view of the logic utilization on the FPGA: the two main colors presented correspond to the redundancy of the application logic programmed on the FPGA.

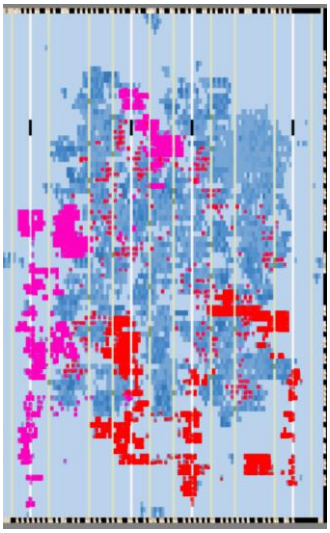

Figure 8: Use of FPGA logic blocks

4.2 Need of specific CAD Tools for developing I&C function

During the design phase we have encountered several issues:

- Some of the elementary blocks were missing in the library so we need to design and test them.
- The necessity to use the FPGA CAD tool was a bit restrictive compared to other PLC suppliers CAD tools. For instance it is impossible to have a real-time display of a FPGA value when the FPGA is programmed and run.
- No real-time tuning mode and no incremental compilation was provided, which has led to long time delays for each change of the control system.

5 CONCLUSION AND PROSPECTS

This design of a control system on a FPGA-based platform has enabled to highlight the specificities and some potential risks of the FPGA technology for certification, means of verification, and the use of a FPGA specific CAD tool.

A coming major update of the FPGA platform will allow the use of floating point elementary blocks and will introduce a supplier specific CAD tool with new features.

Our work program on this platform is not over: we will compare the use of floating point and fixed point methods on the FPGA-based PLC, test some unit-level formal verification tools.

6 ACKNOWLEDGMENTS

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7 REFERENCES

1. **IEC 62566:2012** Nuclear power plants - Instrumentation and control important to safety - Development of HDL-programmed integrated circuits for systems performing category A functions