An automatic Input/Output Test Experience of FPGA based Logic Controller with I/O Stimulator

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ABSTRACT

This paper describes an automatic testing approach instead of a traditional manual test for an FPGA-based Logic Controller (FLC). It mainly describes an automatic testing of FLC using an I/O stimulator with the initiated manual action. The FLC was developed by Doosan Heavy Industry and KAERI in S. Korea. We also developed a test-bed like I/O stimulator for a burning test based on the operational scenario. Signal sources from the I/O stimulator contain an analog input, an analog output, a digital input and a digital output, a programmable power supply, an RS232C serial interface, and a dual port Ethernet interface. LabVIEW Programming was used for the automatic testing. The FLC consists of a general processor module (FPM-01), a complex processor module (FPM-02), analog input modules (FAI-01), analog output modules (FAO-01), digital input modules (FDI-01), digital output modules (FDO-01), a data link module (FDL-01), and a network module (FNW-01). Among these, in this paper, automatic digital I/O testing and automatic analog I/O testing are described. In addition, for the accuracy of the automatic testing, two graphic recorders are used. One is the output results of general processor based testing, and the other is the output results of complex processor based testing. These are different company products. Redundancy recording was found in the test results. The test results were synchronized internally with the existing I/O stimulator and externally with two graphic recorders. Calibrations of all of the equipment were made before the system testing. Before the testing started, a test plan and the test procedure were set up in advance, and we performed test scenario-based automatic functional testing for the FLC as the qualification process. It can be several executed depending on the scenario and conditional parameters of the test. For validation of the accuracy and reliability in our automated test, manual testing was also performed. Manual tests were conducted in two ways. The first one was a manual test using Fluke 754 and Fluke 715. The other one was using embedded manual features of the I/O stimulator. By performing the automatic input and output testing using the I/O stimulator, the time and expense of FLC testing can be reduced significantly compared with a conventional manual test. We rechecked the automatic test results using Fluke-754 manually.

Key Words: FLC, I/O, Stimulator, Signal Generator, Graphic Recorders, Functional Test, Performance Test, System Test

1 INTRODUCTION

The purpose of developing a test-bed for system testing is to save time and effort from functionality and performance tests. We developed a test-bed for a burning test based on an operational scenario. The hardware, software, and man-machine-interface (MMI) are fundamental parts of the test-bed. Signals generated from the test-bed contain an analog input, an analog output, a digital input, and a digital output. Using LabView programming, we established the fact that the test-bed that can generate signal sources consisting of a triangle wave, sign wave, and step-wise signal. The test-bed can control not only the real-time condition parameters, but also the weighted signal test. The test-bed can provide a solution for the time discrepancy between the input signal and resulting value during the synchronization process.

The sequence of automatic system testing is in the order shown below.

o Target for FPGA-based logic controller

o Testing approach

- Functional and performance based testing

- Identifying the test items, selection of test cases, and test execution

o System configuration and test environment

o Test scenarios, pass/fail criteria

o Test procedures and test results

1.1 Test environment for FPGA-based safety-grade logic controller

The FPGA-based safety-grade logic controller consists of a sub-rack, a bus module, a power module, a general processor module, a complex processor module, an analog input module, an analog output module, a digital input module, a digital output module, a data link module, and a network communication module. Figure 1 shows the conceptual connection diagram of the FLC system test using the I/O simulator. The I/O stimulator, which is a signal generator, generates a signal and sends it to the FLC. The test application in the FLC will run and return the test results to the I/O stimulator. The test results are recorded in two types, one is called a "two graphical recorder," which records the results as they are. The other receives the returning signals from the I/O stimulator and compares them to make a decision as to whether they should PASS or FAIL. A loopback approach is used to automatically run the previously defined test cases the designated number of times. The hardware and software of the I/O stimulator were self-developed for the test facility. Manual or automatic mode can be utilized with the I/O stimulator.

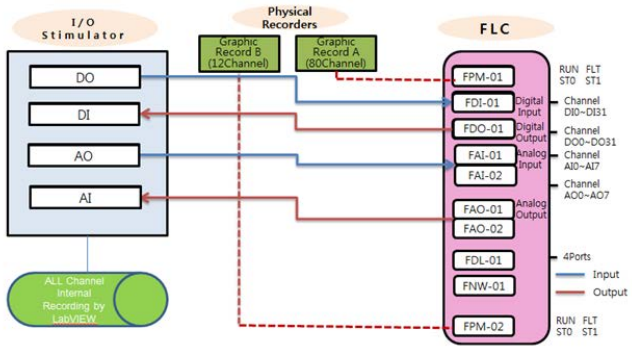
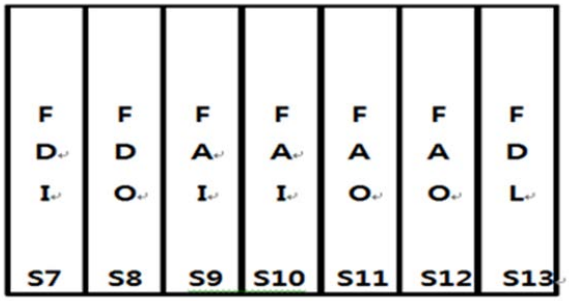


Figure 1. Configuration of automatic testing

1.1.1 General Processor based System Test

The general processor-based system test consists of 32 digital inputs and 32 digital outputs, that is, a total 64 points. The analog has 16 inputs and 16 outputs, i.e., a total of 32 inputs. The slot numbers and card configuration mappings are shown in Figure 2. The automatic test-bed facility is shown in Figure 3. For a general processor-based system test, testing scenarios are implemented so that digital signals and analog signals are combined and mapped without any input/output channels overlapping.



<Figure 2> Configuration of general processor based system test

<Figure 3> FLC system test environment

1.1.2 Complex operation based system test

The complex processor-based system test consists of eight digital inputs, eight digital outputs, and a total of 16 points {CH00 to CH07 (Digital), CH00 to CH03 (Analog)}. The analog has four inputs and four outputs in total. Compared with a general processor, the digital is 1/4, and the analog is 1/2, and thus a minimum function is performed as a countermeasure when the general processor is disabled as a single loop. In normal cases, we can use multiple functions simultaneously in a single loop with normal operations. If the input/output is mapped for these tests, because the digital has 8 channels and the analog has 4 channels, four operational test scenarios are configured, as shown in Table 1, without overlapping any input/output channels. The sequence of test scenarios consists of the external input to the internal bus to the complex processor module and the external output to the external data link.

[Table 1] Complex processor based test scenario

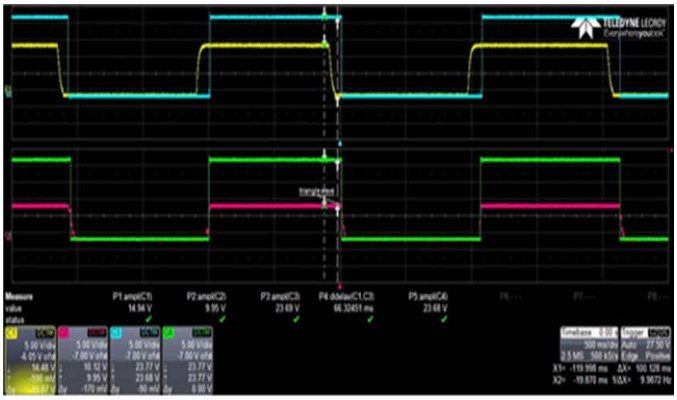
NO	Input channel	Output channel	Comments
1	FDI CH00	FAO CH02	cross
2	FDI CH01	FAO CH03	cross

3	FDI CH02	FDO CH02	
4	FDI CH03	FDO CH03	
5	FDI CH04	FDO CH04	
6	FDI CH05	FDO CH05	
7	FDI CH06	FDO CH06	
8	FDI CH07	FDO CH07	
9	FAI CH00	FAO CH00	
10	FAI CH01	FAO CH01	
11	FAI CH02	FDO CH00	cross
12	FAI CH03	FDO CH01	cross

1.2 Performance Test Results of FPGA-based Safety-grade Logic Controller

All input and output scenarios, digital output from the digital input, analog output from the analog input, digital output from the analog input, and analog output from the digital input were tested according to the test plan and procedure. When the data link was tested together with its own self loopback, the test values were measured using the response time to the change the value by giving a triangular wave signal and a Pick-to-Pick signal, respectively. The system tests for a general processor-based scenario and complex-based scenario were automatically performed using a self-manufactured I/O stimulator. All test results confirmed that they responded within 100ms, as shown in Figures 4 and Figure 5.

<Figure 4> Functional test result



<Figure 5> Performance test result

2 CONCLUSIONS

We tested the functionality, response time, and load balancing to verify the FPGA-based safety-grade logic controller to be used as a safety system platform in nuclear power plants. All of the tests were automatically performed using an I/O stimulator. An FPGA-based safety-grade logic controller was developed and executed under the system test plan and system test procedure based on the software requirements specification (SRS) in order to meet the higher-level requirements.

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