RADIATION HARDENED SUCCESSIVE-APPROXIMATION ADC WITH ERROR DETECTION CIRCUITS

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ABSTRACT

For several decades, radiation-hardened-by-design (RHBD) techniques have been developed to meet the design requirements of irradiating environment in nuclear power plants. Improvements on the circuit side for radiation sensors in performance, chip size, and radiation hardening ability have been adopted in current plant systems; however, next generation reactors and/or preparation for severe events in existing reactors require advanced circuit structures that can provide relatively long viability in harsh conditions.

In order to maintain performances of electronics in high radiating environments, we propose to develop a small-area, low resource-overhead data-converter architecture that is immune to radiation impact events, an architecture that includes three kinds of novel radiation-hardened (rad-hard) designs for each analog and digital circuit in an ADC structure: a) error detectable tri-state buffer for flip flop against DSET, b) error detection storage in flip flop against SEU, and c) analog algorithm for the analog parts of an SAR ADC. The novel ADC architecture including the three RHBD techniques was implemented in a standard 180 nm CMOS technology with a 1.8 V supply voltage. Simulation results show that the techniques can successfully recognize errors induced by radiation impact events. The static power consumption was 123 μW with the sampling rate 36 MS/s and resolution of 8 bits. The performances could be highly advanced under fine-tune designs.

Key Words: Harsh Environment, NPP, RHBD, SAR ADC, SEE, SEU

1 INTRODUCTION

Analog-to-digital converters (ADCs) are essential components to be protected by radiation-hardened-by-design (RHBD) techniques in high radiation environments, for instance, nuclear power plants for monitoring normal operation and preparing against severe accidents, as well as military and space sensing systems. The non-destructive single-event effect (SEE) can affect digital logic blocks in a circuit by flipping the data state, a condition known as a single-event upset (SEU) [1-4]. In addition to digital blocks, the analog part of the circuit is also threatened by a single-event transient (SET) which can contaminate the amplitude, the duration, and the linearity of an analog signal [5-6]. Since most ADCs have both analog and digital blocks in their architectures, SEEs can produce significant errors to a system that includes radiation intolerant ADCs. Therefore, refined RHBD techniques are needed for radiation-tolerant applications.

For many years, RHBD circuits have been developed and adapted from traditional ADC/DAC architectures. One common method is to utilize redundancy in an important block to preserve the correct data. This technique performs a voting process to produce a correct output when any one of the duplicated systems fails due to a SEE. For example, B. Olson applied the redundancy technique, formally termed the triple modular redundancy (TMR), to comparators which is a salient component in a pipelined ADC [7]. Moreover, a dual-path hardening technique implemented on a multiplying digital-to-analog converter circuit (MDAC) and a comparator circuit results in significant radiation hardening in the pipelined ADC architecture. Other methods use various error detection and correction (EDAC) algorithms adding redundant bits in the storage components to detect and correct errors at the system level [8].

These methods have been successfully applied to electronic devices in various space, nuclear, and scientific applications; however, all of the techniques lead to performance penalties in speed, area and resolution by adding TMR, voting circuits, and extra bits for EDAC methods. The multiplication of circuits in a rad-hard component increases the occupied area in an integrated circuit in the form of transistors, capacitors, and resistors, the parasitic capacitance and resistance from which reduces the overall performance of the system [9]. This performance penalty is particularly unwelcome for radiation tolerant applications because they generally demand high performance designs in terms of speed, resolution, and power. Even though high performance can be increasingly delivered by the process development in sub-micron technology, errors induced by radiation impacts increase in effect for smaller component size because smaller charges used in the state-of-art integrated chip technology are more vulnerable to induced charges generated by radiation-impact events.

In this work, three novel RHBD techniques are presented for elements in analog and digital blocks that are potentially at risk from SETs and SEUs. An entire architecture of successive-approximation (SAR) ADC including the new RHBD techniques deliver a high speed of at least 36 Ms/s and 8 bit resolution without latency. The RHBD techniques are fully compatible with standard integrated circuit processes.

2 CONVENTIONAL SAR ADC

The successive-approximation (SAR) ADC is an architecture that can satisfy the required specifications regarding sampling frequency and resolution without latency. Fig. 1 shows the basic diagram of the SAR ADC. The SHA keeps the analog input signal during 1 clock cycle conversion without latency. First, the comparator determines the most significant bit (MSB) by comparing the output of the SHA with the reference value from the DAC, a digital result that is stored in a resister in the digital block. For the next bit determination, the control logic changes the DAC to produce different reference values and the comparator determines the next bit with the changed reference value. The process continues until all of the bit values have been determined. This SAR ADC architecture operates in 1 sampling clock cycle, the consequence of which is no pipeline delay or latency. Analog-to-digital converters (ADCs) are essential components to be protected by radiation-hardened-by-design (RHBD) techniques in high radiation

Another advantage of the SAR ADC is the availability of the high quality resolution of 14 bits as recently published [14-15]. The capacitors that form the DAC can be manufactured with high accuracy and linearity by well-developed photolithography processes in standard microelectronic fabrication. The fine grained capacitors not only yield high bit resolution, but they are also robust to temperature variations better than 1 ppm/^{0}C (parts per million for a 1 Celsius change), a characteristic that is a huge advantage for nuclear, space, defense, and scientific applications.

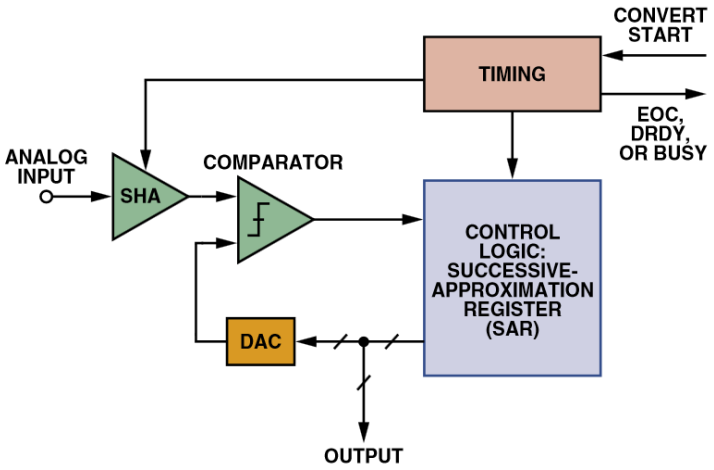

Figure 1. Basic successive-approximation (SAR) ADC.

3 RHBD SAR ADC

For designing radiation hardened circuits, single event transients (SETs) and single event upsets (SEUs) are of primary concern because they are the main phenomena that cause malfunctions in a system by contaminating the data transition and flipping stored bits. SETs can be divided in digital SETs (DSETs) and analog SETs (ASETs). While SEUs primarily threaten the bit integrity in data storage and are relatively easy to solve via system level recovery methods such as EDAC and TMR (at the expense of circuit resources), SETs must be handled intricately because a signal is contaminated during data transition. In order to mitigate the threats presented from SETs and SEUs, three solutions are proposed: a) a modified flip flop for the digital circuits in the control logic of the SAR ADC, b) a data comparison technique in digital storage producing errors by SEUs, and c) a way to detect transition errors by ASETs in the DAC of the SAR ADC.

3.1 RHBD flip-flop for DSET in digital blocks

In fact, errors caused in transition are difficult to catch because of the temporal and spatial uncertainty associated with radiation impact events. Prior work uses either EDAC for a system level treatment or TMR for a voting method modality [7-8]. However, these methods are resource-intensive: TMR requires a three times expansion in area for redundancy circuits and EDAC needs more calculation time as well as redundancy bit-storage units. In order to reduce this hardware and software burden, an in situ error detection flip-flop that one of us has already developed, can be utilized for the radiation hardened ADC [11]. This technique allows a system to recognize a delayed signal as an error due to SET and recovery the error by a roll-back system by recalculating the failed clock period.

Fig. 2 shows the detailed schematic of the modified flip-flop. First considering the standard flip-flop, when a signal arrives at the node D from the previous stage, the first inverter drives current from the power rail into the storage comprised of two inverters in a feedback loop through the transmission gate. The modified latch combines the transmission gate and the inverter into a tri-state buffer to monitor any charge sharing effects at one of the virtual power nodes, named VVDD and VVSS, resulting in the detection of a late arriving signal as shown in Fig. 3. Once one of the virtual nodes, VVDD or VVSS, is triggered by a late signal due to a radiation impact, the ADC rolls back the previous stage for one clock cycle to redo the incorrect calculation. Even though this method requires more redundancy clock cycles, it can be easily implanted into the proposed SAR ADC because the digital clock is usually very high speed (up to GHz range) while the targeted sampling rate of the SAR ADC is 36 Ms/s.

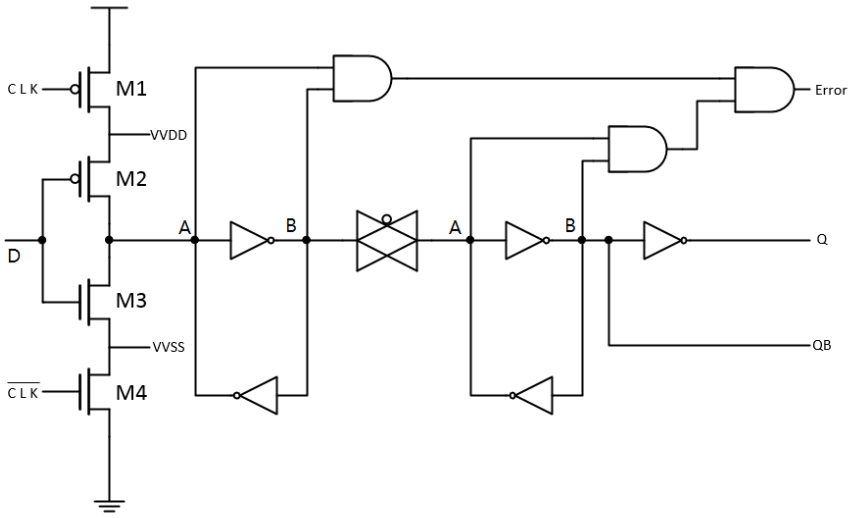

Figure 2. Modified D flip flop for the digital circuits in the control logic against DSET and SEU.

Table I. Transistor size of the modified flip flop

Device	Size	
	W(nm)	L(nm)
M1	440	180
M2	440	180
M3	220	180
M4	220	180

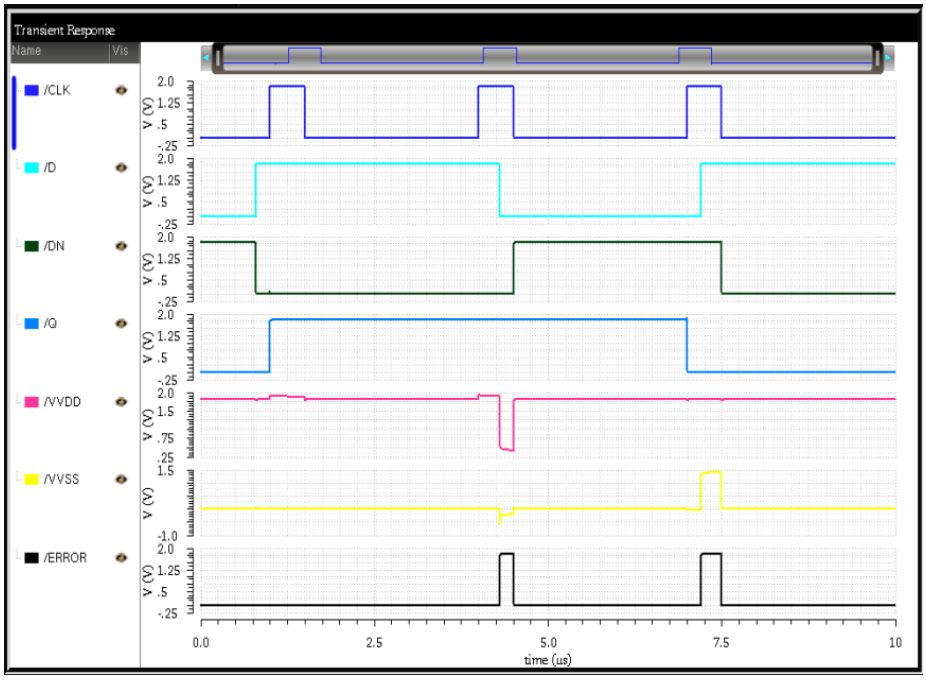

Figure 3. Feasibility test of the RBHD D flip flop against DSET.

3.2 RHBD flip-flop for SEU in digital blocks

Aside from SETs, single event upsets (SEUs) are another primary error mode in radiation-impacted digital circuits. Even though SET effects can be mitigated by the proposed in situ error detection flip-flop described in the last section, SEUs can cause a severe problem in the feedback storage of the flip-flop. Even a single storage data flipped by a SEU in an ADC can lead to totally different digitized results at the output if the flipped data is close to most significant bit. In order to correct the error, a simple NAND gate is proposed, which is inserted into the feedback storage, as shown in Fig. 2. The NAND gate, consisting of only four additional transistors, has small area overhead and power consumption because it's not operating if there are no radiation errors.

The SEU error detector operates as follows. Initially, let us assume that the node A in Fig. 4 is 0 and the node B is 1 logically (1.8 V in this 180 nm SPICE model). When a quanta of radiation impacts node A, the voltage of the node A increases with the amount of charge induced by the radiation impact. The rapidly increasing charges pulls up the voltage of the node A while the voltage of node B is decreased. That is, the bit of stored data is flipped. Fortunately, the inserted NAND gate can sense the charge-induced flipping and generate a negative signal ('/error/' in Fig. 4) when both nodes A and B are high.

3.3 RHBD Algorithm for SET in analog blocks

The proposed flip-flop containing two error-detection solutions can correct the malfunctions of digital circuits caused by radiation impact events. In contrast, analog parts in an ADC are hard to protect from SET effects since many circuit components such as comparators and amplifiers are scattered in the whole ADC. For pipelined ADCs in particular, the ADC requires a multitude of analog circuits between the stages, ultimately occupying a larger area than that of digital circuits, which are usually fabricated with minimal size. Fortunately, analog circuits in the SAR ADC architecture are a relatively small part of the entire system. The control-logic and timing blocks in Fig. 1 indicate digital circuits to control the reference voltages generated by the DAC for the comparator. The analog circuits consist of only one comparator, a capacitor ladder in the DAC and some switches. In other words, three blocks: the SHA, a comparator, and the DAC in Fig. 1, can be implemented in one analog block for the SAR ADC structure, as shown in Fig. 5. Namely, if an error-correcting solution can handle the single analog block having two input nodes (in differential system, otherwise, one tract for a single-ended architecture) properly, then the entire ADC can achieve a radiation hardened design on the analog part as well as digital part as we mentioned in previous sections.

The concept adds one more comparator adjacent to the original comparator by separating the input nodes, but reversing the signs at the input of comparators. Since the sign is reversed for differential inputs, the outputs of the two comparators should be the same, 1 or 0. If a SET occurs on one of the nodes via radiation impact and induces the voltage of the negative node to drive larger than that of the positive node, the output of the comparator on the minus node would alone be flipped. Since the two outputs of the comparators are different, we can recognize an error induced from a SET event and fix the error through roll back system.

For a more detailed example, assuming there is a 2 bit SAR ADC in Fig. 6 with differential input pairs, a configuration preferred in modern circuit architectures compared to single-ended inputs because of greater noise reduction capability. The range of analog input is from -1V to 1V and ±0.2V inputs come into the ADC. The ADC performs something like a binary search, usually determining 1 bit from each cycle starting with the MSB. At the rising sampling clock, the analog input is stored in a capacitor and the digital controller sets up the first reference with 0V for determining the most significant bit (MSB). The comparator, then, decides whether the input is larger than the reference, and outputs a 1 as the MSB. During the second digital clock, the controller changes the reference to 0.5V to determine the next bit, a 0, because the reference voltage is larger than the input voltage. Finally, the two bit digitized output

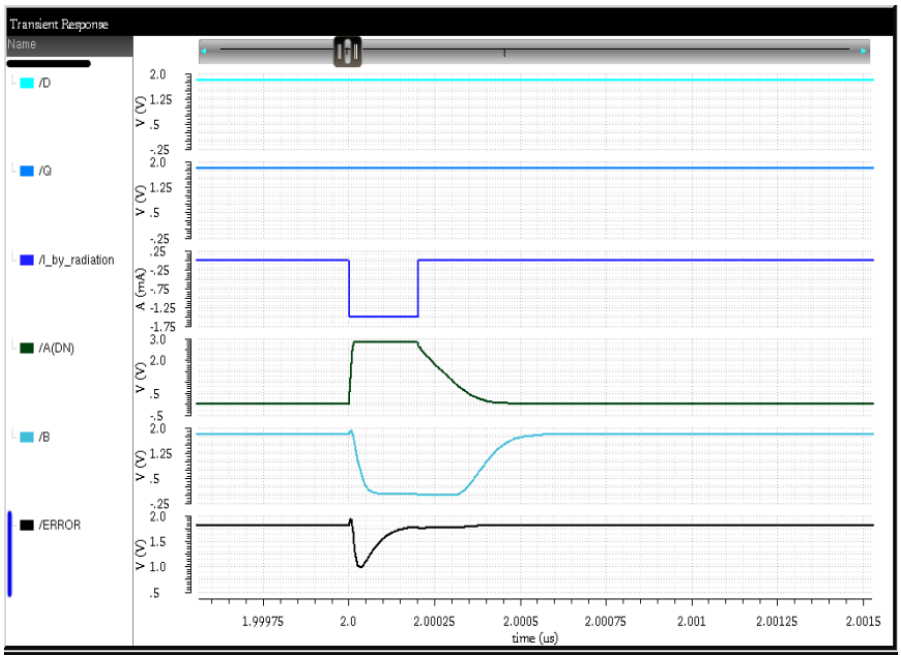

Figure 4. Feasibility test of the RBHD D flip flop against SEU.

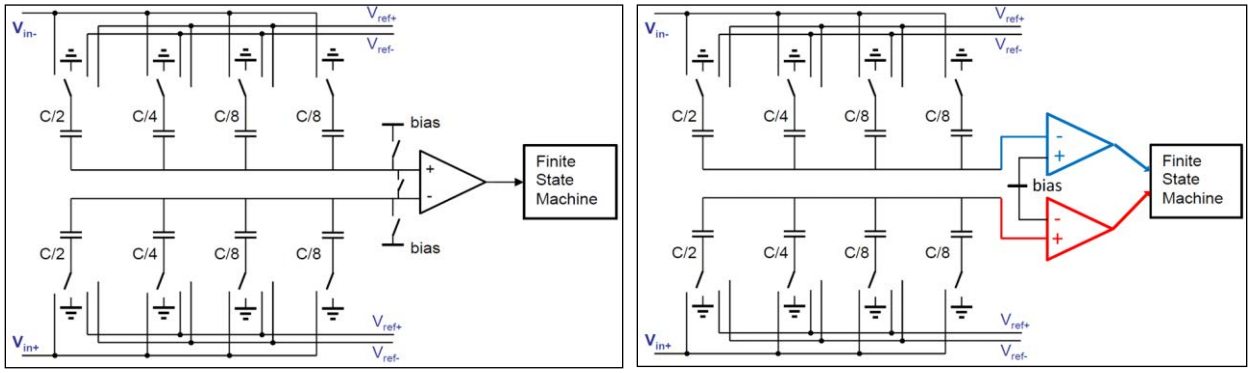

Figure 5. Practical implementation schematic of the analog blocks for a RHBD SAR ADC architecture.

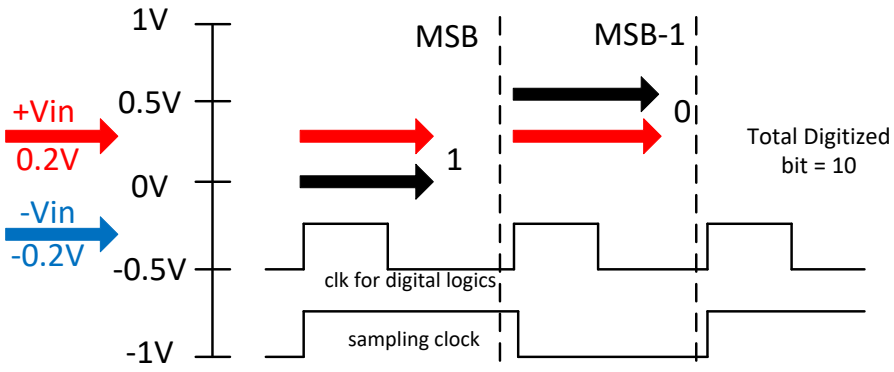

Figure 6. 2 bit SAR ADC example with a clock for the digital control block and a sampling clock for sample and hold of analog input signal.

generates 10 after one sampling clock period. Similarly, the minus input, -Vin, will have the same digitized result of 10 because the minus input goes into the minus sign of the following comparator.

The feasibility test was performed with a ramp input while observing output digital codes as shown in Fig. 7. The zoom-in part (inserted figure in Fig. 7) is clearly showing different values (light blue and dashed green) from each output of the comparators after a radiation event (blue line) injected into the one of input nodes, proving the novel architecture against SET.

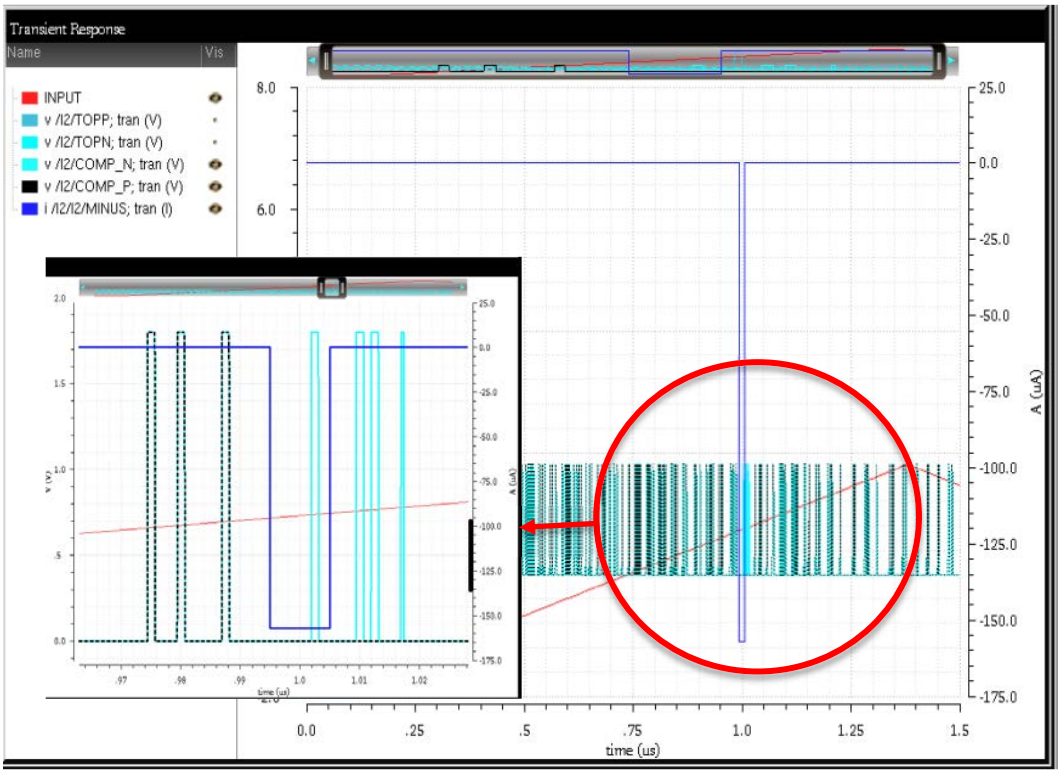

Figure 7. Feasibility test of the proposed ADC when a radiation event occurred in one node of ADC inputs.

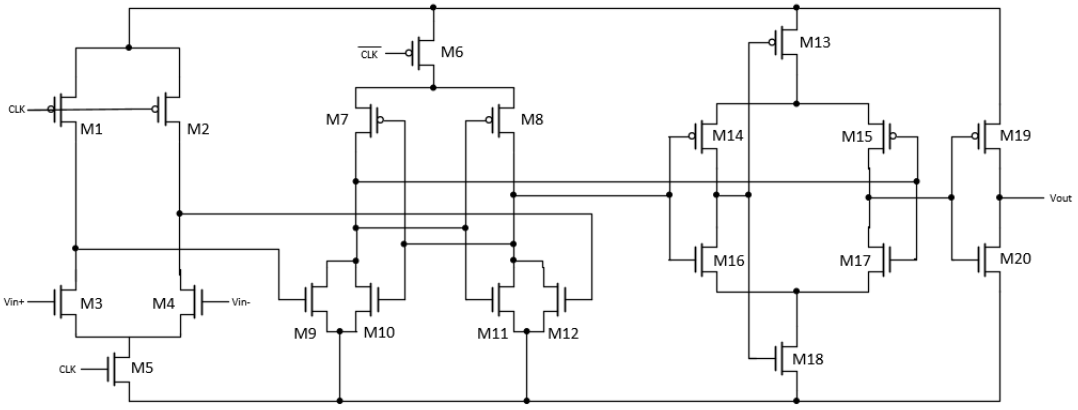

Figure 8. Detailed schematic of the comparator in the ADC

Table II. Transistor size of the comparator in the ADC

Device	Size	
	W(um)	L(um)
M1	0.88	0.36
M2	0.88	0.36
M3	4	0.36
M4	4	0.36
M5	70	0.36
M6	4	0.36
M7	4	0.36
M8	4	0.36
M9	0.4	0.36
M10	1	0.36

Device	Size	
	W(um)	L(um)
M11	1	0.36
M12	0.4	0.36
M13	1.76	0.36
M14	1.76	0.36
M15	1.76	0.36
M16	1	0.36
M17	1	0.36
M18	1	0.36
M19	3.36	0.36
M20	1.76	0.36

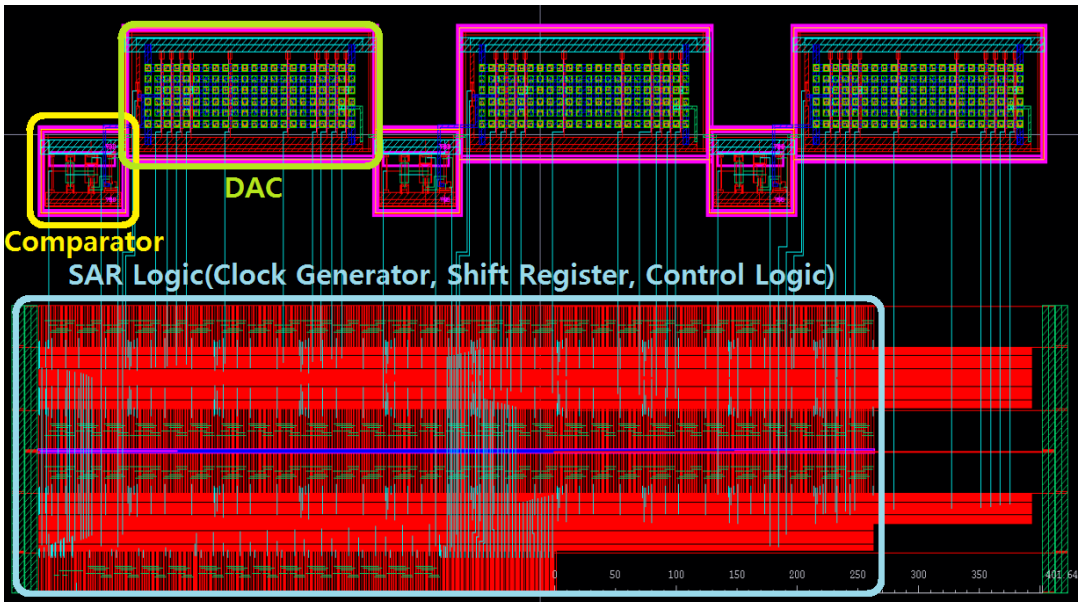

Figure 9. Layout of the entire RHBD SAR ADC

Table III. Specification of the RHBD SAR ADC

Process	0.18 um CMOS
Power	123 uW
Supply	1.8 V
Resolution(bit)	8 bit
Sampling Rate	36 MS/s

4 CONCLUSION

For surviving electronics in harsh radiation conditions such as preparation for severe events and/or Gen IV reactors with radioactive colorants, we proposed the three RHBD techniques: 1) in situ error detection flip-flops, 2) hardened storage flip-flops, and 3) the error detection algorithm for both of analog and digital circuits. The transistor level design was proven by electrically modeled radiation impact events with 36 MS/s and 8 bit resolution at 1.8V supply. These three RHBD techniques based on a rollback mechanism requires enough marginal clocks for the digital controller. In this scheme, the key issue is how many spare clock cycles are needed to correct for increasing rates of SEU and SET events due to high radiation-rates, the consequence of which are many errors called multi-cell upsets (MCU) or multi-bit upsets (MBU). Even though the speed of the digital clock frequency is limited by fundamental reasons on the manufacturing process and the material features, a well-balanced design with minimum size of transistors can operate beyond a GHz. For instance, if the clock frequency for the digital blocks is 1 GHz, then there are 40 clock cycles available for the digital controller in the ADC, assuming a sampling rate of 25 Ms/s. The other target specification, 14 bit resolution for precise particle-detector conversion, utilizes 14 clock cycles within one sampling rate. Thus, 26 marginal clock cycles are available for the rollback system.

5 ACKNOWLEDGMENTS

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